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Docket No.: 57454-206

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Yasuhiro NUNOMURA

Serial No.:

Group Art Unit:

Filed: August 14, 2001

Examiner:

For: MULTIPROCESSOR SYSTEM CONTROLLING FREQUENCY OF CLOCK INPUT TO
PROCESSOR ACCORDING TO RATIO OF PROCESSING TIMES OF PROCESSORS,
AND METHOD THEREOF



INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Serial No.:

Each non-English reference is accompanied by an English Abstract.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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| INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449) | | | | ATTY. DOCKET NO. 57454-206 | | SERIAL NO. | |
| | | | | APPLICANT Yasuhiro NUNOMURA | | | |
| | | | | FILING DATE August 14, 2001 | | GROUP | |
| U.S. PATENT DOCUMENTS | | | | | | | |
| EXAMINER'S INITIALS | PATENT NO. | DATE | NAME | CLASS | SUBCLASS | FILING DATE | |
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| FOREIGN PATENT DOCUMENTS | | | | | | | |
| EXAMINER'S INITIALS | PATENT NO. | DATE | COUNTRY | CLASS | SUBCLASS | Translation | |
| | | | | | | Yes | No |
| | 8-6681 | 1/12/1996 | Japan (w/ English Abstract) | | | | |
| | 5-28116 | 2/5/1993 | Japan (w/ English Abstract) | | | | |
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| OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | | |
| | "Computer Architecture: Design and Performance", B. Wilkinson, April 30, 1994, p. 210. | | | | | | |
| | "Real-Time Task Scheduling for a Variable Voltage Processor", T. OKUMA et al., The Journal of The Institute of Electronics, Information and Communication Engineers, C Vol. J83-C No. 6, June 2000, pp. 454-462. | | | | | | |
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| EXAMINER | | | | DATE CONSIDERED | | | |

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.